**256× 4b的RAM：**

module RAM\_256(A,Din,Dout,clk,str,sel,ld,clr);

input [7:0] A;//??

input [3:0] Din;

input clk,str,sel,ld,clr;

output reg[3:0] Dout;

integer i;

reg [3:0] data[255:0]; //?256?????????????4????

initial begin

Dout = 4'bz;

end

always@(posedge clk or posedge clr)

begin

if(sel == 0) begin Dout = 4'bxxxx; end

else

begin

if(clr == 1)

begin

for(i = 0; i < 255; i = i+1)

data[i] = 0;

end

else if(str == 1)

begin

data[A] = Din;

end

else if(ld == 1)

begin

Dout = data[A];

end

else begin Dout = 4'bz; end

end

end

endmodule

**256× 4b的RAM测试文件：**

module RAM\_256(A,Din,Dout,clk,str,sel,ld,clr);

input [7:0] A;//??

input [3:0] Din;

input clk,str,sel,ld,clr;

output reg[3:0] Dout;

integer i;

reg [3:0] data[255:0]; //?256?????????????4????

initial begin

Dout = 4'bz;

end

always@(posedge clk or posedge clr)

begin

if(sel == 0) begin Dout = 4'bxxxx; end

else

begin

if(clr == 1)

begin

for(i = 0; i < 255; i = i+1)

data[i] = 0;

end

else if(str == 1)

begin

data[A] = Din;

end

else if(ld == 1)

begin

Dout = data[A];

end

else begin Dout = 4'bz; end

end

end

endmodule